

### **REMARKS/ARGUMENTS**

The Applicants originally submitted Claims 1-20 in the application. In the present response, the Applicants have amended independent Claims 1 and 15 in response to a 35 U.S.C. §101 rejection. Support for the amendment can be found, for example, in paragraph 25 of the original specification. Claims 1-20 are currently pending in the application.

#### **I. Rejection of Claims 1-7 and 15-20 under 35 U.S.C. §101**

The Examiner has rejected Claims 1-7 and 15-20 under 35 U.S.C. §101 for being directed to non-statutory subject matter. In response, the Applicants have amended independent Claims 1 and 15 to render this rejection moot. Accordingly, the Applicants respectfully request the Examiner to withdraw the §101 rejection and allow issuance of Claims 1 and 15 and Claims dependent thereon.

#### **II. Rejection of Claims 1-2, 4-9 and 11-14 under 35 U.S.C. §103**

The Examiner has rejected Claims 1-2, 4-9 and 11-14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,937,190 to Gregory in view of U.S. Patent No. 5,568,644 to Nelson, *et al*, and further in view of Practical C Programming, 3<sup>rd</sup> Edition, O'Reilly, August 1997 to Qualline. The Applicants respectfully disagree.

The Examiner recognizes Gregory does not teach or suggest an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers. (*See Examiner's Action*, pages 3-4.) To cure this deficiency, the Examiner relies on Nelson. More specifically, the Examiner asserts that the Interrupt

Source Tree (IST) of Nelson discloses an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers. (See Examiner's Action, page 4.) Even assuming the IST is such an intermediate graph, the Examiner does not assert and has not shown where the IST is generated by parsing a High-Level Design Language (HDL) file. On the contrary, the cited sections of Nelson disclose the IST structure but do not provide any teaching or suggestion that the IST was generated by parsing an HDL file. (See column 1, line 51; column 3, lines 9-15 and lines 31-44; and Figure 1A.) Thus, neither Nelson nor Gregory teach or suggest parsing a HDL file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers as recited in independent Claim 1.

The Examiner asserts that one skilled in the art would find it obvious to combine the teachings of Gregory with the teachings of Nelson to arrive at parsing a HDL file to generate an intermediate graph as recited in Claim 1. (See Examiner's Action, page 4.) Nelson, however, does not provide an enabling disclosure for parsing a HDL file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers. As stated in *Elan Pharm.*, a "disclosure in an assertedly anticipating reference must provide an enabling disclosure of the desired subject matter; mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation." (See MPEP 2121.01 citing *Elan Pharm., Inc. v. Mayo Found. For Med. Educ. & Research*, 346 F.3d 1051, 1054, 68 USPQ2d 1373, 1376 (Fed. Cir. 2003).) More

specifically addressing an obviousness rejection, *In re Kumar* states that “in order to render an invention unpatentable for obviousness, the prior art must enable a person of ordinary skill to make and use the invention.” (See *In Re Kumar*, No. 04-1074, (Fed. Cir. 2005), citing *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989).)

Nelson fails to provide an enabling disclosure of *parsing a HDL file* to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers. As noted by the Examiner, Gregory also fails to provide such an enabling disclosure. Thus, the cited combination of Gregory and Nelson fails to provide an enabling disclosure of parsing a HDL file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers. Oualline has not been cited to cure this deficiency of Gregory and Nelson but teach another limitation of Claim 1. (See Examiner's Action, page 5.) As such, the cited combination does not provide a *prima facie* case of obviousness of independent Claim 1 and Claims dependent thereon. Analogously, the cited combination does not a *prima facie* case of obviousness of Claim 8 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection with respect to Claims 1-2, 4-9 and 11-14 and allow issuance thereof.

### **III. Rejection of Claims 3, 10 and 15-20 under 35 U.S.C. §103**

The Examiner has rejected Claims 3, 10 and 15-20 under 35 U.S.C. §103(a) as being unpatentable over Gregory and Nelson in view of Oualline, and further in view of Perl & LWP, O'Reilly, June 2002 to Burke.

As discussed above the cited combination of Gregory, Nelson and Oualline does not provide a *prima facie* case of obviousness for independent Claims 1 and 8. The cited combination of Gregory, Nelson and Oualline, therefore, also does not provide a *prima facie* case of obviousness of independent Claim 15. Burke has not been cited to cure the noted deficiencies of the cited combination but to teach an HTML traversable tree representation based on a mathematical tree. (See Examiner's Action, page 12.) Thus, the cited combination of Burke with Gregory, Nelson and Oualline also fails to provide a *prima facie* case of obviousness of independent Claims 1, 8 and 15 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection with respect to Claims 3, 10 and 15-20 and allow issuance thereof.

#### IV. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



J. Joel Justiss  
Registration No. 48,981

Dated: August 16, 2007

P.O. Box 832570  
Richardson, Texas 75083  
(972) 480-8800